SEP 1 4 2004 and Attorney Docket No.: MTI-31607

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Teck Kheng Lee

Serial No.

10/050,507

Confirmation No.

7687

Filing Date

January 16, 2002

For

Elimination of RDL Using Tape Base Flip Chip on Flex for Die Stacking

Group Art Unit

2812

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

I hereby certify that, on the date shown below, this correspondence is being:

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Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97/98

Sir:

In compliance with Applicant's duty of disclosure as set forth in 37 C.F.R. §1.56, listed on the attached Form PTO-1449 are those patents and other publications known to Applicant which may be considered material to the patentability of the claims of the above-identified application.

Applicant respectfully requests that the Examiner consider the documents listed on the attached Form PTO-1449, that these references be made of record in the present application, and that an initialed copy of the attached Form PTO-1449 be returned to the undersigned in accordance with MPEP 609.

Respectfully submitted,

Dated:

September 9, 2004

Kristine M. Strodthoff, Reg. No. 34259

WHYTE HIRSCHBOECK DUDEK S.C.

555 East Wells Street, Suite 1900 Milwaukee, Wisconsin 53202-3819

(414) 273-2100

Customer No.: 31870

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE Alexandria, VA 22313

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

ATTY. DOCKET NO.

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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

Examiner		Document	Publication		Int'l	Sub-	Translation
Initial		Number	Date	Country	Class	Class	(Yes/No)
	Al	2000-183082	06-30-00	JP	HOIL	21/566	Abstract
	A2	2001077294	03-23-01	JP	H01L	25/065	Yes
	A3	99/65282	12-16-99	WO	H05K	1/11	N/A

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)

Examiner		
Initial		Non-Patent Document
	BI	Copy of Australian Patent Office, Search Report, 30 May 2003, 4 pages.
	B2	Al-sarawi, S. et al., "A Review of 3-D Packaging Technology," Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging, Vol 21, Issue 1, Feb. 1998, pp. 2-14.
	В3	Andros, F. et al., "TBGA Package Technology," Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging, Vol. 17, Issue 4, Nov. 1994, pp. 564-568.
	B4	Clot, Ph. et al., "Flip-Chip on Flex for 3D Packaging," 1999. 24 th IEEE/CPMT, 18-19 Oct. 1999, pp. 36-41.
	B5	Ferrando, F. et al., "Industrial Approach of a Flip-Chip Method Using the Stud-Bumps With a Non-Conductive Paste," <i>Adhesive Joining and Coating Technology in Electronics Manufacturing</i> , 2000. Proceedings. 4 th International Conference on, 18-21, June 2000, pp. 205-211.
	В6	Gallagher, C. et al., "A Fully Additive, Polymeric Process for the Fabrication and Assembly of Substrate and Component Level Packaging," <i>The First IEEE International Symposium on Polymeric Electronics Packaging</i> , 26-30, Oct. 1997, pp. 56-63.
	В7	Geissinger, J. et al., "Tape Based CSP Package Supports Fine Pitch Wirebonding," <i>Electronics Manufacturing Technology Symposium</i> , 2002, IEMT 2002, 27 th Annual IEEE/SEMI International, 17-18 July 2002, pp. 41-452.
	B8	Hatanaka, H., "Packaging Processes Using Flip Chip Bonder and Future Directions of Technology Development," <i>Electronics Packaging Technology Conference</i> , 2002. 4 th , 10-12, Dec. 2002, pp. 434-439.
	В9	Haug, R. et al., "Low-Cost Direct Chip Attach: Comparison of SMD Compatible FC Soldering with Anisotropically Conductive Adhesive FC Bonding," <i>IEEE Transactions on Electronics Packaging Manufacturing</i> , Vol. 23, No. 1, Jan 2000, pp. 12-18.

Examiner Initials	Date Considered
EXAMINER: Initial if citation considered, whether or not citation	on is in conformance with MPEP 609; Draw line through citation if not
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Initial		Non-Patent Document
	B10	Isaak, H. et al., "Development of Flex Stackable Carriers" IEEE Electronic Components and
		Technology Conference, 2000 Proceedings 50th, 5/21/2000-5/24/2000, Las Vegas, NV, USA, pp. 378-84, IEEE Catalog No: 00CH37070.
	B11	Kloeser, J. et al., "Fine Pitch Stencil Printing of Sn/Pb and Lead Free Solders for Flip Chip
		Technology," IEEE Transactions of CPMT - Part C, vol. 21, No. 1, 1998, pp. 41-49.
	B12	Kheng et al., "Enhancement of Moisture Sensitivity Performance of a FBGA," Proceedings of
		International Symposium on Electronic Materials & Packaging, 2000, pp. 470-475.
	B13	Li, L. et al., "Stencil Printing Process Development for Flip Chip Interconnect," <i>IEEE Transactions</i>
		Part C: Electronics Packaging Manufacturing, Vol. 23, Issue 3, July 2000, pp. 165-170.
	B14	Lyons, A. et al., "A New Approach to Using Anisotropically Conductive Adhesives for Flip-Chip
		Assembly, Part A, " IEEE Transactions on Components, Packaging, and Manufacturing
		Technology, Vol. 19, Issue 1, March 1996, pp. 5-11.
	B15	Teo, Y. et al., "Enhancing Moisture Resistance of PBGA," Electronic Components and Technology
		Conference, 1998. 48 th IEEE, 25-28 May 1998, pp. 930-935.
	B16	Teutsch, T. et al, "Wafer Level CSP using Low Cost Electroless Redistribution Layer," Electronic
	}	Components and Technology Conference, 2000. 2000 Proceedings. 50th, 21-24 May 2000, pp.
	D17	Pages: 107-113.
	B17	"The 2003 International Technology Roadmap for Semiconductors: Assembly and Packaging", pp. 1-22
	B18	Tsui, C, et al. "Pad Distribution Technology for Flip Chip Applications", 1998 Electronic
	р 16	Components and Technology Conference, pp. 1098-1102
	B19	Xiao, G. et al., "Reliability Study and Failure Analysis of Fine Pitch Solder-Bumped Flip Chip on
	619	Low-Cost Flexible Substrate Without Using Stiffener," IEEE, 2002. Proceedings 52 nd , 28-31 May
		2002, pp. 112-118.
_	L	2002, pp. 112-116.

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